An Electrolytic-Capacitor-Free Single-Phase High-Power Fuel Cell Converter With Direct Double-Frequency Ripple Current Control

Xiaohu Liu, *Member, IEEE*, and Hui Li, *Senior Member, IEEE*

***Abstract*—This paper proposes a direct double-frequency ripple current control in a single-phase high-power fuel cell converter that can achieve low-frequency ripple-free input current without using large electrolytic capacitors. To eliminate the double-frequency ripple current disturbance introduced by the single-phase inverter load, a proportional–resonant controller is developed to achieve an extra high control gain at designed resonant frequency. This high gain can be viewed as the virtual high impedance for blocking the double-frequency ripple energy propagation from inverter load to fuel cell stack. More particularly, the proposed control system can realize the utilization of all capacitive ripple energy sources in the system by regulating all the capacitors to have large voltage swing. In addition, this voltage swing is synchronized to keep real-time balancing of the transformer primary- and secondary-side voltages. As a result, the zero-voltage-switching operation for all switching devices in the dc–dc stage can be guaranteed. The controller design guidelines are derived based on the system small-signal model. The experimental results are presented to validate the theoretical analysis and proposed technology.**

***Index Terms*—Current-fed three-phase dc–dc converter, direct double-frequency ripple current control, electrolytic capacitor free, fuel cell, zero voltage switching (ZVS).**

I. Introduction

FUEL cells are emerging as a promising energy source for mobile and power generation applications due to their high efficiency, high reliability, and low emissions of regulated pollutants [1]–[5]. Fuel cell system requires the electrical isolation between the low-voltage output of the fuel cell stack and the high-voltage dc bus for protection [6]. The high-frequency-link (HFL) power converter [7]–[11] is therefore being widely applied in fuel cell system [12]–[18] since it provides high-frequency galvanic isolation and benefits a large reduction in the size and weight of the isolation transformer.

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X. Liu is with the High Frequency Power Electronics Laboratory, GE Global Research Center, Schenectady, NY 12309 USA (e-mail: xiaohu.L@ge.com).

H. Li is with the Electrical and Computer Engineering Department, Florida A&M University–Florida State University College of Engineering, Tallahassee, FL 3231 USA (e-mail: hli@caps.fsu.edu).

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One of the key issues in fuel cell system is that the full cell current low-frequency ripple exhibits a hysteresis behavior and results a thermal issue among stacks [19]. A straightforward solution is to apply the bulky electrolytic capacitor as the energy buffer to reduce the ripple current. However, the electrolytic capacitor decreases the system lifetime and increases the system volume and cost [20]. Therefore, to suppress the low-frequency ripple without using electrolytic capacitors is crucial to fuel cell systems. Recently, some literature have researched on the methods to mitigate fuel cell low-frequency ripple current without using electrolytic capacitors [14]–[18]. However, those solutions cannot be directly applied for the high-power fuel cells, which usually require the multiphase dc–dc converter as the front end.

In fuel cell high-power applications, research has been focused on the three-phase dc–dc-converter-based power conditioning system since it offers better performance over its single-phase counterpart in terms of higher power density, lower switching device current stress, smaller size of passive components, and so on [21]–[25]. The type of three-phase dc–dc converter could be either current fed or voltage fed. Based on the study performed in [23]–[25], current-fed topology is better suited to low-voltage high-current fuel cell application where high voltage step-up ratio is required. Moreover, the current-fed topology benefits from the direct and precise input current control.

Previous research on three-phase dc–dc converters for fuel cells mainly focused on the high efficiency and high power density. The method to reduce the fuel cell low-frequency ripple current has been seldom discussed. Reference [26] presents the voltage-fed high-power fuel cell converter, which consists of a V6 converter [22] and a full-bridge inverter. It proposes the ripple current mitigation method by using a current-loop control within the existing voltage loop to mitigate the fuel cell low-frequency ripple. However, the large electrolytic capacitor is still required as an energy buffer. Up to date, there have been no published literature that research the methods to reduce the low-frequency ripple current in the current-fed three-phase dc–dc-converter-based fuel cell system.

This paper proposes a three-phase current-fed interleaved-structure-based HFL fuel cell system. Compared with other three-phase dc–dc-converter-based fuel cell systems, the unique advantages of our proposal fall into the following three aspects. First, a direct double-frequency ripple current control based on the current-fed three-phase HFL converter is proposed to achieve the low-frequency ripple-free input current. Second,

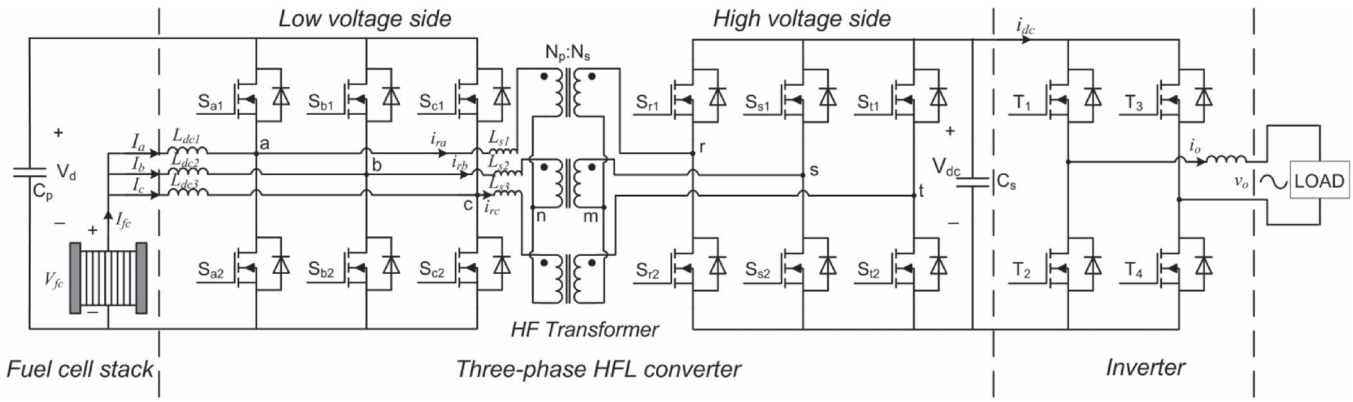

Fig. 1. Proposed two-stage HFL-based high-power fuel cell power conditioning system.

the proposed method is to apply a control-oriented ripple current mitigation strategy without adding any extra circuit components. The small film capacitor can be adopted to replace the bulky electrolytic capacitor. Third, the control system can realize the full utilization of capacitive ripple energy sources in the proposed fuel cell system, which benefits a further reduction in dc-bus capacitance. Moreover, with all those contributions listed above, the zero-voltage-switching (ZVS) operation of all switching devices in the dc–dc stage can still be maintained without adding any extra circuits.

The rest of this paper is organized as follows. The proposed fuel cell system description and its low-frequency ripple circuit modeling are presented in Section II. Section III describes the proposed direct double-frequency ripple current control system. To illustrate the proposed control system design principle, the three-phase HFL converter ZVS conditions and its small-signal model are also derived. The experimental verification is provided in Section IV. Conclusions are summarized in Section V.

II. Proposed Fuel Cell System Low-Frequency Ripple Circuit Modeling

A. Proposed Fuel Cell System Description

Fig. 1 shows the proposed two-stage HFL-based high-power fuel cell system. The system consists of a current-fed three-phase HFL converter with an isolated Y-Y connected high-frequency (HF) transformer and an inverter. The three-phase HFL converter power flow is controlled by the phase shift angle φ between the active switches on the low-voltage side (LVS) and the high-voltage side (HVS). The converter can be operated either in the boost mode or in the buck mode. In this paper, the converter is operated in boost mode for fuel cell application. The boost function is achieved by the dc inductors ($L_{\rm dc1}$, $L_{\rm dc2}$, and $L_{\rm dc3}$) and three half-bridges on the LVS. The leakage inductors (L_{s1}, L_{s2}, and L_{s3}) are the energy transfer element for each phase.

The major features of this three-phase HFL converter have been studied in [27]. However, the method to reduce the input double-frequency ripple current caused by the inverter load has not been discussed. This paper's research focus is to study the direct double-frequency ripple current control of this three-phase HFL converter when connecting a single-phase inverter load.

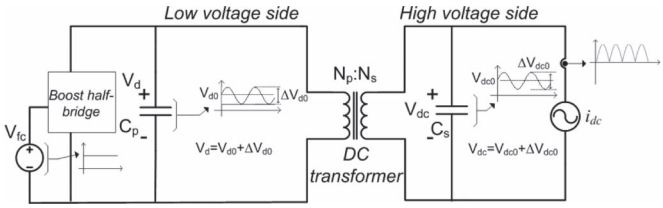

Fig. 2. Equivalent ripple circuit model of the proposed fuel cell system.

B. Equivalent Ripple Circuit Modeling of the Proposed Fuel Cell System

Fig. 2 shows the equivalent ripple circuit model of the proposed fuel cell system. $V_{\rm fc}$ is the fuel cell stack voltage. If fuel cell current has negligible low-frequency ripple current, $V_{\rm fc}$ is the constant voltage. The dc–dc converter can be simplified as an ideal dc transformer since its switching frequency is much larger than the system ripple frequency [26]. The inverter load is modeled as a double-frequency pulsation current source $i_{\rm dc}$. As shown, both the LVS dc-bus voltage V_d and the HVS dc-bus voltage $V_{\rm dc}$ have the relatively large voltage swing. This control is designed based on the following three aspects. First, large voltage variation of $V_{\rm dc}$ leads to small HVS dc-bus capacitor C_s, which makes it viable to replace the electrolytic capacitor with a film capacitor. This has already been explained in [15]. Second, if real-time balancing of transformer primary- and secondary-side voltages can be maintained by synchronizing V_d with primary-referred $V_{\rm dc}$, the three-phase HFL converter can always maintain the ZVS operation. This will be further explained in the next section. Third, voltage variation on both LVS and HVS dc buses makes both the primary- and secondary-side capacitive energy sources (C_p and C_s, as shown in the circuit in Fig. 2) to provide the ripple energy required by the inverter load. According to the fuel cell system ripple energy calculation performed in [15], the circuit ripple energy balancing shown in Fig. 2 can be expressed in

$$C_p V_{d0} \Delta V_d + C_s V_{\rm dc0} \Delta V_{\rm dc} = \frac{P_{\rm load}}{\omega_{\rm load}} \tag{1}$$

where V_{d0} and ΔV_{d0} are the LVS dc-bus average voltage and voltage variation (peak to peak), respectively. $V_{\rm dc0}$ and $\Delta V_{\rm dc0}$ are the HVS dc-bus average voltage and voltage variation (peak

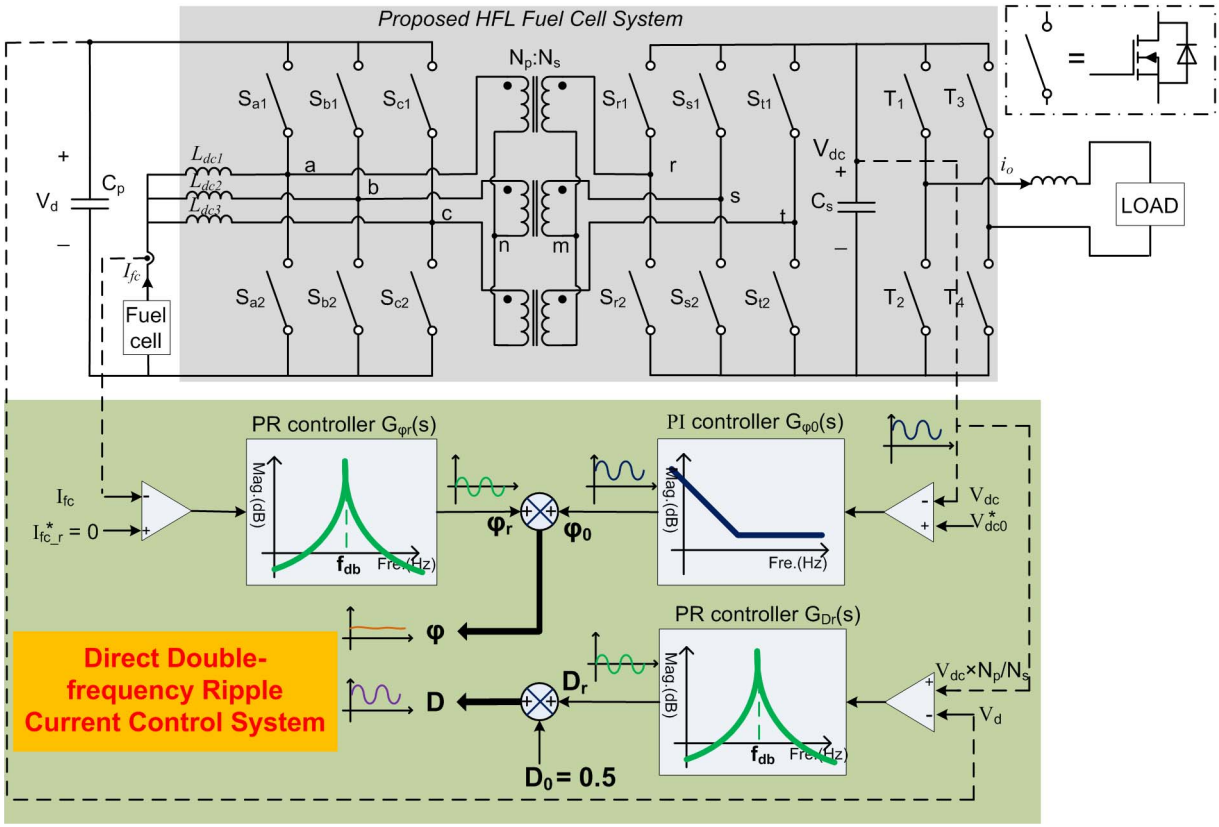

Fig. 3. Proposed direct double-frequency ripple current control system diagram.

to peak), respectively. $P_{\rm load}$ is the load real power, and $\omega_{\rm load}$ is the load angular frequency.

As illustrated in (1), the proposed fuel cell system can make full utilization of system capacitive ripple energy. This is a unique advantage compared with the voltage-fed fuel cell converter. Since the voltage-fed fuel cell system connects the LVS dc-bus capacitor C_p directly to the fuel cell stack [26], therefore, the capacitive ripple energy of C_p is not able to be utilized.

III. Direct Double-Frequency Ripple Current Control System and Design

A. Direct Double-Frequency Ripple Current Control System Description

Fig. 3 presents the proposed direct double-frequency ripple current control system diagram. The proposed control system includes duty cycle control and phase shift control. The duty cycle $D = D_0 + D_r$, as illustrated. First, the dc component of D, D_0 is set to be 0.5. This is because the three-phase HFL converter has the optimized operation efficiency at 50% duty cycle [27]. Second, the ripple component of D, D_r is generated by synchronizing the LVS dc-bus voltage V_d with the primary-referred HVS dc-bus voltage $V_{\rm dc}$. The purpose is to real-time balance the transformer primary- and secondary-side voltages in order to ensure the ZVS operation of all switching devices in the dc–dc converter. The detailed analysis of ZVS operation will be explained in the next Section III-B. The proportional–resonant (PR) controller is adopted for $G_{Dr}(s)$ to regulate the swing of V_d. The design guideline of controller $G_{Dr}(s)$ will be explained in Section III-C. As shown in Fig. 3, the real-time primary-referred $V_{\rm dc}$ is employed as the voltage reference. The LVS dc-bus voltage V_d is equal to $V_{\rm fc}/D$ due to the LVS half-bridge boost function. $V_{\rm fc}$ is a constant value if $I_{\rm fc}$ has no low-frequency ripple. Therefore, D will contain a double-frequency ripple in order to keep V_d synchronized with primary-referred $V_{\rm dc}$, which has the double-frequency variation.

The phase shift angle $\varphi = \varphi_0 + \varphi_r$, as illustrated. First, the dc component of φ, φ_0 is generated by regulating $V_{\rm dc0}$ to meet the inverter modulation requirement so the inverter can generate the required ac voltage. A proportional–integral (PI) controller $G_{\varphi 0}(s)$ is adopted to regulate $V_{\rm dc0}$. The voltage reference $V^*_{\rm dc0}$ is a constant dc value. The feedback $V_{\rm dc}$ consists of a constant dc value $V_{\rm dc0}$ and a double-frequency ripple $\Delta V_{\rm dc}$. The control objective of $G_{\varphi 0}(s)$ is only to regulate the dc component of $V_{\rm dc}$ to follow $V^*_{\rm dc0}$. Therefore, a PI controller can be selected. Due to the relatively large $\Delta V_{\rm dc}$ in the feedback, the double-frequency component will be generated in the controller output φ_0. In addition, this double-frequency component will be reflected on the fuel cell current if the inverter load ripple energy is propagated into the fuel cell stack through the HFL converter.

In order to block the ripple energy propagation from inverter load to fuel cell stack, a direct double-frequency ripple current controller $G_{\varphi r}(s)$ is developed. The PR controller is employed for $G_{\varphi r}(s)$ since the PR controller can generate an extra high control gain at its resonant frequency. This high gain can be viewed as the virtual high impedance for blocking the ripple energy. As illustrated, the current ripple references $I^*_{\rm fc\_r}$ is 0.

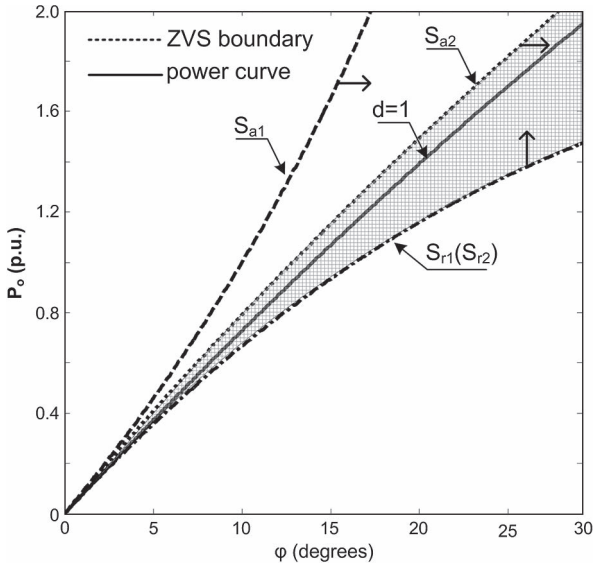

Fig. 4. Scaled power curves and ZVS boundaries of S_{a1}, S_{a2}, S_{r1}, and S_{r2} at $D = 0.5$ with $L_{\rm dc1}/L_{s1} = 13.3$.

The real-time $I_{\rm fc}$, which consists of a dc component and a double-frequency ripple, is directly used for feedback. This is because the controller $G_{\varphi r}(s)$ is designed to be immune to the dc component and to only respond to the double-frequency component. As a result, φ_r, i.e., the output of $G_{\varphi r}(s)$, is a double-frequency component. The design guideline of $G_{\varphi 0}(s)$ and $G_{\varphi r}(s)$ will be explained in Section III-C. The inverter control adopts the traditional single-phase dual-loop $d-q$ vector control [14].

B. ZVS Operation Analysis With Large Swing Bus Voltage

The basic principle of ZVS operation is to gate on the incoming device while the antiparallel diode is conducting. To analyze the ZVS conditions, the variable d is defined in [27], which is listed in (A.1). "$d = 1$" means that V_d matches with primary-referred $V_{\rm dc}$. If $d = 1$, the ZVS conditions are always satisfied for HVS switches and LVS upper switches (S_{a1}, S_{b1}, S_{c1}, as shown in the circuit in Fig. 3). For LVS lower switches (S_{a2}, S_{b2}, S_{c2}, as shown in the circuit in Fig. 4) ZVS conditions, the ratio of dc inductor divided by leakage inductor is another key factor. Small ratio leads to large inductor current ripple, which results in large soft switching operation region for LVS lower switches. However, the large current ripple leads to large inductor core loss and conduction loss. It is therefore a tradeoff design. In this paper, this ratio is selected to be 13.3. Due to the converter symmetric property, each phase switches on the same position have the same ZVS conditions. The soft switching conditions of phase A switches are selected for study. According to [27], the soft switching conditions for phase A LVS and HVS switches are listed in (A.2). The three-phase HFL output power and 1 per unit (p.u.) base power are given in (A.3) and (A.4), respectively. Based on (A.2)–(A.4), the scaled power curves and ZVS boundaries of phase A switches at $D = 0.5$ with $L_{\rm dc1}/L_{s1} = 13.3$ are shown in Fig. 4. As illustrated, the shaded area is a soft switching region. If $d = 1$ control can be achieved, the operation can be always maintained within the soft switching region. This explains why V_d is real-time synchronized with primary-referred $V_{\rm dc}$ in the proposed control system.

C. Controller Design Principle With Large Swing Bus Voltage

In order to design the controller $G_{\varphi r}(s)$, $G_{\varphi 0}(s)$, and $G_{Dr}(s)$, the three-phase HFL converter small-signal model needs to be studied. References [29] and [30] have developed the average model of the studied three-phase converter. Due to the symmetric property, the modeling of the three-phase HFL converter can be treated as the model of a single-phase half-bridge converter. Phase A is selected to illustrate the average model that is given in (A.5). However, the small-signal model with respect to the inverter load current disturbance has not been studied in [29] and [30]. Therefore, the small-signal model considering the inverter load current disturbance is given in the following. By introducing the small perturbations around the nominal operation point in the model given in (A.5), the small-signal model of a phase A half-bridge converter could be developed as follows:

$$\begin{cases} L_{\rm dc1}\dfrac{d\widetilde{i}_a}{dt} = \widetilde{v}_{\rm in} - D\widetilde{v}_d - V_d\widetilde{D} \\ C_p\dfrac{d\widetilde{v}_d}{dt} = D\widetilde{i}_a + I_a\widetilde{D} - \dfrac{\phi(4\pi-3\phi)}{18\pi\omega L_{s1}}\widetilde{v}_{\rm dc} - \dfrac{V_{\rm dc}(4\pi-6\phi)}{18\pi\omega L_{s1}}\widetilde{\varphi} \\ C_s\dfrac{d\widetilde{v}_{\rm dc}}{dt} = -\widetilde{i}_{\rm dc} + \dfrac{\phi(4\pi-3\phi)}{18\pi\omega L_{s1}}\widetilde{v}_d + \dfrac{V_d(4\pi-6\phi)}{18\pi\omega L_{s1}}\widetilde{\varphi} \end{cases} \tag{2}$$

where $i_{\rm dc}$ is the inverter double-frequency pulsation current, as shown in the circuit in Fig. 3.

Therefore, the state-space equations can be expressed as follows:

$$\begin{cases} \begin{bmatrix} \dot{\widetilde{i}}_a \\ \dot{\widetilde{v}}_d \\ \dot{\widetilde{v}}_{\rm dc} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{D}{L_{\rm dc1}} & 0 \\ \frac{D}{C_p} & 0 & \frac{-\phi(4\pi-3\phi)}{\rm con1} \\ 0 & \frac{\phi(4\pi-3\phi)}{\rm con2} & 0 \end{bmatrix} \cdot \begin{bmatrix} \widetilde{i}_a \\ \widetilde{v}_d \\ \widetilde{v}_{\rm dc} \end{bmatrix} \\ \quad + \begin{bmatrix} \frac{1}{L_{\rm dc1}} & 0 & \frac{-V_d}{L_{\rm dc1}} & 0 \\ 0 & \frac{-V_{\rm dc}(4\pi-6\phi)}{\rm con1} & \frac{I_a}{C_p} & 0 \\ 0 & \frac{V_d(4\pi-6\phi)}{\rm con2} & 0 & \frac{-1}{C_s} \end{bmatrix} \cdot \begin{bmatrix} \widetilde{v}_{\rm in} \\ \widetilde{\varphi} \\ \widetilde{D} \\ \widetilde{i}_{\rm dc} \end{bmatrix} \\ \widetilde{v}_{\rm dc} = [\,0 \quad 0 \quad 1\,] \cdot [\,\widetilde{i}_a \quad \widetilde{v}_d \quad \widetilde{v}_{\rm dc}\,]^T \\ \widetilde{i}_a = [\,1 \quad 0 \quad 0\,] \cdot [\,\widetilde{i}_a \quad \widetilde{v}_d \quad \widetilde{v}_{\rm dc}\,]^T \end{cases} \tag{3}$$

$$\begin{cases} \dot{\widetilde{x}} = A\widetilde{x} + B\widetilde{u} \\ y = C\widetilde{x} \end{cases} \quad A = \begin{bmatrix} 0 & -\frac{D}{L_{\rm dc1}} & 0 \\ \frac{D}{C_p} & 0 & \frac{-\phi(4\pi-3\phi)}{\rm con1} \\ 0 & \frac{\phi(4\pi-3\phi)}{\rm con2} & 0 \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{1}{L_{\rm dc1}} & 0 & \frac{-V_d}{L_{\rm dc1}} & 0 \\ 0 & \frac{-V_{\rm dc}(4\pi-6\phi)}{\rm con1} & \frac{I_a}{C_p} & 0 \\ 0 & \frac{V_d(4\pi-6\phi)}{\rm con2} & 0 & \frac{-1}{C_s} \end{bmatrix} \tag{4}$$

$$\begin{cases} y_1 = \widetilde{i}_a, C_1 = [\,1 \quad 0 \quad 0\,] \\ y_2 = \widetilde{v}_d, C_2 = [\,0 \quad 1 \quad 0\,] \\ y_3 = \widetilde{v}_{\rm dc}, C_3 = [\,0 \quad 0 \quad 1\,] \end{cases} \tag{5}$$

where con1 $= 18\pi\omega L_{s1}C_p$, and con2 $= 18\pi\omega L_{s1}C_s$.

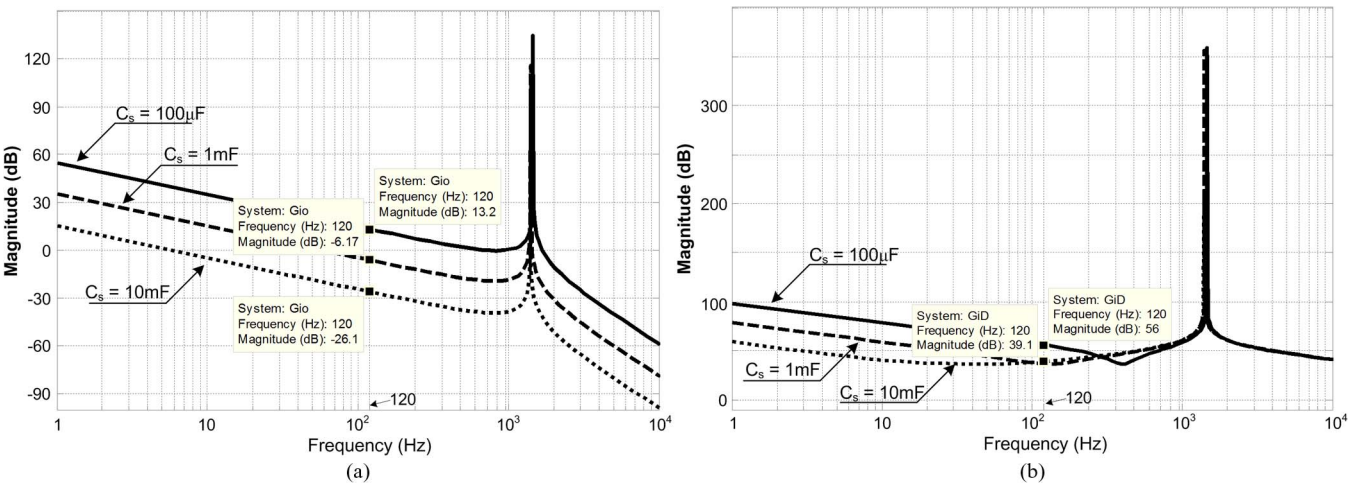

Fig. 5. Open-loop transfer function bode diagrams with different values of C_s. (a) $G_{io}(s)$. (b) $G_{iD}(s)$.

Based on the small-signal model shown in (3)–(5), the transfer function matrix from input factors to the input current can be obtained in (6), shown at the bottom of the page. The inverter load current disturbance to input current transfer function $G_{io}(s)$, the control-to-input current transfer function $G_{i\varphi}(s)$, and the duty cycle disturbance to input current transfer function $G_{iD}(s)$ can be calculated and are given in (7)–(9), respectively, shown at the bottom of the page.

Fig. 5 shows the open-loop $G_{io}(s)$ and $G_{iD}(s)$ bode diagrams based on (7) and (9) with different values of C_s. The circuit parameter values of (7) and (9) are as follows: $L_{\rm dc1} = 14.6\ \mu$H, $L_{s1} = 1.1\ \mu$H, $C_p = 220\ \mu$F, and $f_s = 40$ kHz. The nominal operation point is $\varphi = 0.056\pi$, $V_d = 20$ V, $V_{\rm dc} = 200$ V, and $I_a = 16$ A. The low-frequency component of $i_{\rm dc}$ is only the 120-Hz ripple current since the inverter outputs 60-Hz ac voltage. Therefore, the 120-Hz response of $G_{io}(s)$ is highlighted. As shown in Fig. 5(a), the response is 13.2 dB with $C_s = 100\ \mu$F, which means that the input current 120-Hz ripple magnitude is 4.57 times of $i_{\rm dc}$ magnitude. The response with $C_s = 10$ mF is only -26.1 dB, which means that the input current 120-Hz ripple magnitude is only 0.05 times of $i_{\rm dc}$ magnitude. This explains why the large dc capacitor is able to suppress the input current double-frequency ripple.

$$\begin{aligned}\widetilde{i}_a(s) &= C_1(sI-A)^{-1}B\widetilde{u}(s)\\ &= G_{iv}(s)\widetilde{v}_{\rm in}(s) + G_{i\phi}(s)\widetilde{\phi}(s) + G_{iD}(s)\widetilde{D}(s) + G_{io}(s)\widetilde{i}_{\rm dc}(s)\end{aligned} \tag{6}$$

$$G_{io}(s) = \left.\frac{\widetilde{i}_a(s)}{\widetilde{i}_{\rm dc}(s)}\right|_{\substack{\widetilde{v}_{\rm in}(s)=0\\ \widetilde{\phi}(s)=0\\ \widetilde{D}(s)=0}} = \frac{-D\phi(4\pi-3\phi)}{sL_{\rm dc1}C_s{\rm con1}\left(s^2+\phi(4\pi-3\phi)^2/({\rm con1con2})+D^2/(C_pL_{\rm dc1})\right)} \tag{7}$$

$$G_{i\varphi}(s) = \left.\frac{\widetilde{i}_a(s)}{\widetilde{\phi}(s)}\right|_{\substack{\widetilde{v}_{\rm in}(s)=0\\ \widetilde{D}(s)=0\\ \widetilde{i}_{\rm dc}(s)=0}} = \frac{C_pD\left(sV_{\rm dc}(4\pi-6\phi){\rm con2}+V_d\phi(4\pi-3\phi)(4\pi-6\phi)\right)}{s\left(s^2C_pL_{\rm dc1}{\rm con1con2}+C_pL_{\rm dc1}\phi(4\pi-3\phi)^2+D^2{\rm con1con2}\right)} \tag{8}$$

$$G_{iD}(s) = \left.\frac{\widetilde{i}_a(s)}{\widetilde{D}(s)}\right|_{\substack{\widetilde{v}_{\rm in}(s)=0\\ \widetilde{\phi}(s)=0\\ \widetilde{i}_{\rm dc}(s)=0}} = \frac{-\left(s^2C_pV_d{\rm con1con2}+sDI_a{\rm con1con2}+C_pV_d\phi(4\pi-3\phi)^2\right)}{s\left(s^2C_pL_{\rm dc1}{\rm con1con2}+C_pL_{\rm dc1}\phi(4\pi-3\phi)^2+D^2{\rm con1con2}\right)} \tag{9}$$

$$\frac{G_{io}(s)}{1+T_r(s)} = \left.\frac{\widetilde{i}_a(s)}{\widetilde{i}_{\rm dc}(s)}\right|_{\substack{\widetilde{i}_{a\_{\rm ref}}(s)=0\\ \widetilde{v}_{\rm in}(s)=0\\ \widetilde{D}(s)=0}} = \frac{G_{io}(s)}{1+G_{\phi r}(s)G_{i\varphi}(s)} \tag{10}$$

$$\frac{G_{iD}(s)}{1+T_r(s)} = \left.\frac{\widetilde{i}_a(s)}{\widetilde{D}(s)}\right|_{\substack{\widetilde{i}_{a\_{\rm ref}}(s)=0\\ \widetilde{v}_{\rm in}(s)=0\\ \widetilde{i}_{\rm dc}(s)=0}} = \frac{G_{iD}(s)}{1+G_{\phi r}(s)G_{i\varphi}(s)} \tag{11}$$

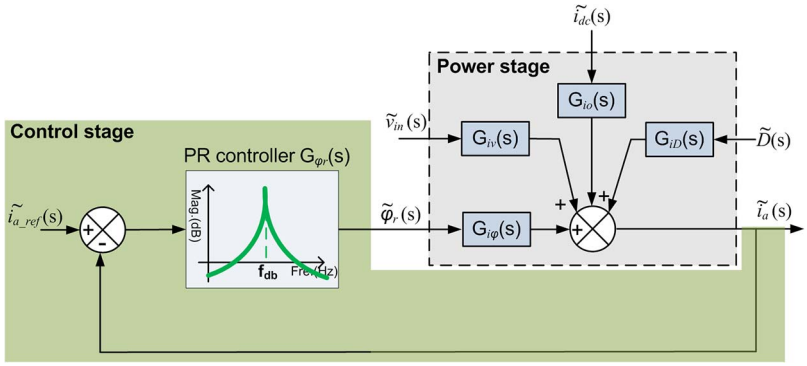

Fig. 6. Phase A input current small-signal model block diagram.

Since the duty cycle D also has the double-frequency ripple as explained in Section III-A, its disturbance to the input current also needs to be studied. As shown in Fig. 5(b), the input current always has a relatively large response to the duty cycle disturbance regardless of C_s value. The response is 39.1 dB with $C_s = 10$ mF, which means that the input current 120-Hz ripple magnitude is 98.86 times of D ripple magnitude. Therefore, this disturbance has to be mitigated if implementing the proposed $d = 1$ varied duty cycle control.

Based on the developed small-signal model, the phase A input current small-signal model block diagram is illustrated in Fig. 6. Therefore, the closed-loop inverter load disturbance and the duty cycle disturbance to the fuel cell current transfer function can be obtained and are given in (10) and (11), respectively, shown at the bottom of the preceding page. As shown, the compensated system has the loop gain $1/(1 + T_r(s))$. This loop gain response at 120 Hz is found to be very small if the proposed controller $G_{\varphi r}(s)$ is designed to have a relatively large response at 120 Hz. As a result, the fuel cell current response to inverter load disturbance and duty cycle disturbance can both be minimized since the low-frequency component of both disturbances only consists of 120-Hz component. The PR controller is therefore selected because it can be designed to have an extra high gain only at its resonant frequency. In addition, this resonant frequency is set to be 120 Hz for the proposed technology.

The PR controller $G_{\varphi r}(s)$ can be expressed by $K_p s/(s^2 + (2\pi f_r)^2)$, where $f_r = 120$. The principle of choosing K_p is to ensure that $G_{\varphi r}(s)$ has negligible dc component response and relatively large resonant frequency response. It is a trade-off design. Fig. 7 shows the bode diagrams of PR controller $G_{\varphi r}(s)$, compensated $G_{io}(s)$, and $G_{iD}(s)$ with $C_s = 100$ μF. K_p is selected to be 0.2. This value is appropriate since the 120-Hz disturbance response is 85.8 dB and the dc component response is smaller than -100 dB, as illustrated in Fig. 7. As

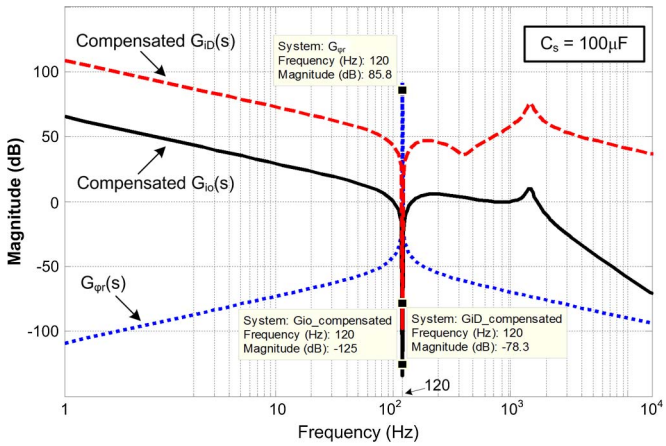

Fig. 7. Bode diagrams of PR controller $G_{\varphi r}(s)$, compensated $G_{io}(s)$, and $G_{iD}(s)$ with $C_s = 100$ μF.

a result, the real-time $I_{\rm fc}$ can be directly used for feedback with respect to zero reference since its dc component response is negligible. The compensated $G_{io}(s)$ and $G_{iD}(s)$ responses to 120-Hz disturbance are -125 and -78.3 dB, respectively. Therefore, the compensated system can theoretically eliminate the fuel cell double-frequency ripple current caused by the inverter load current and duty cycle.

Based on the small-signal model shown in (3)–(5), the transfer function matrix from input factors to the output voltage $V_{\rm dc}$ is given in (12), shown at the bottom of the page. In order to design the controller $G_{\varphi 0}(s)$, control-to-output transfer function $G_{v\varphi 2}(s)$ is calculated and given in (13), shown at the bottom of the page, based on the developed small-signal model. As shown in (13), it has a pair of conjugated right-half-plane zeros. Therefore, the system stability criterion is that the phase margin $\Phi_m = 180^\circ - 2 \times 180^\circ + \langle G_{v\varphi 2}(j2\pi f_c) > 0$, where f_c is the crossover frequency. Fig. 8 shows the bode

$$\begin{aligned}\widetilde{v}_{\rm dc}(s) &= C_3(sI - A)^{-1}B\widetilde{u}(s) \\ &= G_{vv2}(s)\widetilde{v}_{\rm in}(s) + G_{v\varphi 2}(s)\widetilde{\phi}(s) + G_{vD2}(s)\widetilde{D}(s) + G_{vo2}(s)\widetilde{i}_{\rm dc}(s) \qquad (12)\end{aligned}$$

$$G_{v\phi 2}(s) = \frac{(4\pi - 6\phi)\left(s^2 C_p V_d L_{\rm dc1}{\rm con1} - sC_p V_{\rm dc} L_{\rm dc1}\phi(4\pi - 3\phi) + V_d\phi D^2{\rm con1}\right)}{s\left(s^2 C_p L_{\rm dc1}{\rm con1con2} + C_p L_{\rm dc1}\phi(4\pi - 3\phi)^2 + D^2{\rm con1con2}\right)} \qquad (13)$$

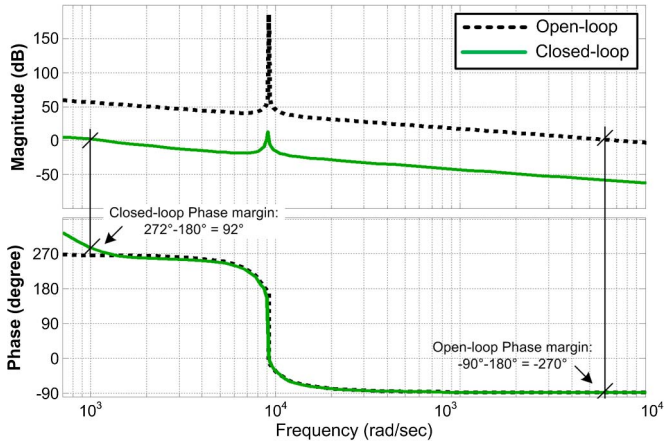

Fig. 8. Bode diagrams of open-loop and closed-loop $G_{v\varphi 2}(s)$ with $C_s = 100\ \mu$F.

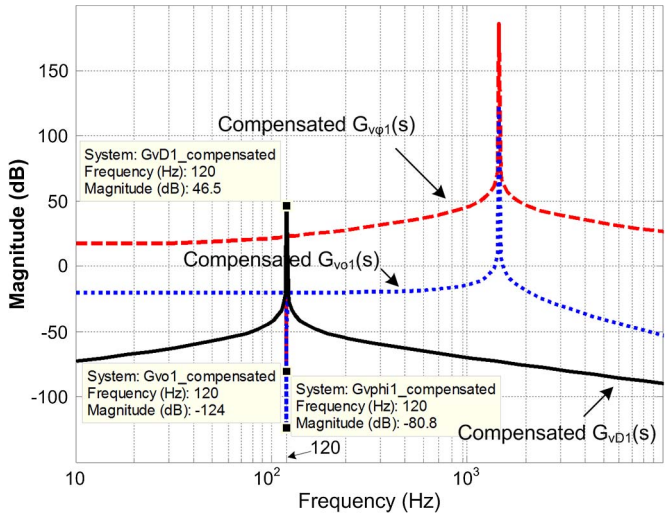

Fig. 9. Bode diagrams of compensated $G_{v\varphi 1}(s)$, $G_{vo1}(s)$, and $G_{vD1}(s)$ with $C_s = 100\ \mu$F.

diagrams of open-loop and closed-loop $G_{v\phi 2}(s)$ with $C_s = 100\ \mu$F. The parameters of (13) are the same as those used in (7). As shown, the system open-loop phase margin $\Phi_m = -270^\circ > 0$. Therefore, the stability of open-loop system is theoretically very poor. However, as explained in [31], all the lossy components add more inertia to the system; thus, the real converter is actually more stable. The $G_{\varphi 0}(s)$ design principle is to ensure the system stability. As shown in Fig. 8, where $G_{\varphi 0}(s) = (1 + 0.001 \times s)/s$, the compensated system phase margin $\Phi_m = 92^\circ < 0$. Therefore, the compensated system is more stable.

The design procedure of controller $G_{Dr}(s)$ is very similar to the design of $G_{\varphi r}(s)$. Therefore, the detailed process will not be repeated here. The $G_{Dr}(s)$ design principle is to ensure that the V_d has the relatively large response at 120 Hz so it can be synchronized with primary-referred V_d to maintain $d = 1$. In addition, the disturbance caused by the phase shift angle φ should be minimized in order to decouple the phase shift controller and the duty cycle controller. The transfer function matrix from input factors to the output voltage V_d is given in (14), shown at the bottom of the page. The phase shift angle disturbance to V_d transfer function $G_{v\phi 1}(s)$, the control-to-output transfer function $G_{vD1}(s)$, and the inverter load current disturbance to V_d transfer function $G_{vo1}(s)$ can be calculated and are given in (15)–(17), respectively, shown at the bottom of the page. The compensated $G_{v\varphi 1}(s)$, $G_{vo1}(s)$, and $G_{vD1}(s)$ bode diagrams are given in Fig. 9 with $G_{Dr}(s) = 0.01s/(s^2 + (2\pi \cdot 120)^2)$. As illustrated in Fig. 9, V_d response at 120 Hz is 46.5 dB, and its response to inverter load and phase shift angle disturbance is -124 and -80.8 dB, respectively. Therefore, the compensated system can theoretically maintain $d = 1$ control and eliminate the inverter load current and phase shift angle disturbance. As a result, the phase shift angle controller and the duty cycle controller can be theoretically well decoupled.

D. Comparison of Proposed Technology Application on Low- and High-Power Fuel Cell Systems

The author has presented the fuel cell low-frequency ripple current mitigation technology based on the current-fed dual-half-bridge dc–dc converter in [14]. However, the proposed method in [14] cannot be directly applied to the high-power fuel cell system. The main reason is that the split capacitors in the dc–dc converter have to take the full load current [13], [14]. It is therefore not suitable for high-power applications. The contribution of this paper is that, based on the previous work in [14], the proposed three-phase HFL-converter-based fuel cell system not only can gain all the benefits presented in [14] in the case of high-power application but also achieve improved performance with regard to the dc capacitor reduction

$$\begin{aligned}\widetilde{v}_d(s) &= C_2(sI - A)^{-1}B\widetilde{u}(s) \\ &= G_{vv1}(s)\widetilde{v}_{\text{in}}(s) + G_{v\varphi 1}(s)\widetilde{\phi}(s) + G_{vD1}(s)\widetilde{D}(s) + G_{vo1}(s)\widetilde{i}_{\text{dc}}(s) \end{aligned} \tag{14}$$

$$G_{v\phi 1}(s) = \frac{-C_p L_{\text{dc1}}(4\pi - 6\phi)\left(sV_{\text{dc}}\text{con2} + V_d\phi(4\pi - 3\phi)\right)}{s^2 C_p L_{\text{dc1}}\text{con1con2} + C_p L_{\text{dc1}}\phi(4\pi - 3\phi)^2 + D^2\text{con1con2}} \tag{15}$$

$$G_{vD1}(s) = \frac{\text{con1con2}(sI_a L_{\text{dc1}} - DV_d)}{s^2 C_p L_{\text{dc1}}\text{con1con2} + C_p L_{\text{dc1}}\phi(4\pi - 3\phi)^2 + D^2\text{con1con2}} \tag{16}$$

$$G_{vo1}(s) = \frac{\frac{L_{\text{dc1}}\phi(4\pi - 3\phi)\text{con2}C_p}{C_s}}{s^2 C_p L_{\text{dc1}}\text{con1con2} + C_p L_{\text{dc1}}\phi(4\pi - 3\phi)^2 + D^2\text{con1con2}} \tag{17}$$

TABLE I
COMPARISON OF PROPOSED TECHNOLOGY APPLICATIONS ON LOW- AND HIGH-POWER FUEL CELL SYSTEMS

		current-fed dual-half-bridge dc-dc converter based fuel cell system [14]	**the proposed three-phase HFL converter based fuel cell system**
dc-dc converter control System	phase-shift control	• regulate the dc-bus average voltage • mitigate the fuel cell current low-frequency ripple	• regulate the dc-bus average voltage, • mitigate the fuel cell current low-freuqency ripple • decouple the duty-cycle control
	duty-cycle control	fixed 50% duty-cycle control	• maintain soft-swithcing opration • decouple the phase-shift control
targeted application		low-power fuel cell application (<3kW), limited by the split capacitors	high-power fuel cell application, benifits from the inter-leaved multi-phase structure.
dc capacitor reduction		limited by the dc-dc converter soft-switching operation. The dc capacitor reduction is 90.4%	not limited by the soft-switching condition. The dc capacitor reduction is 94.3% (The test results are presented in the section IV).
dc-dc converter soft-switching operation		limited range	always be guaranteed

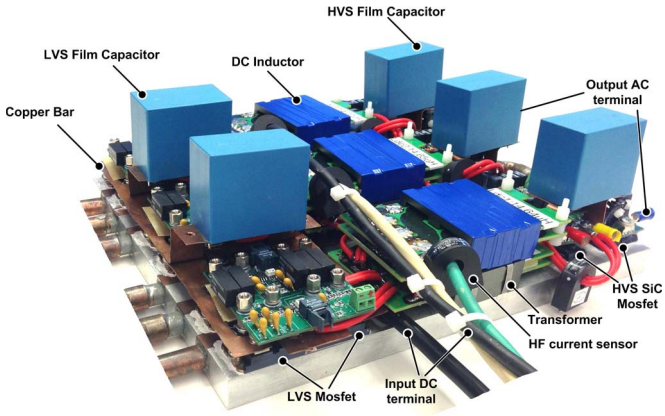

Fig. 10. Proposed three-phase HFL-converter-based fuel cell power conditioning system test bed.

and the dc–dc converter soft switching operation. Table I lists the comparison of proposed technology applications on low- and high-power fuel cell systems. The comparison of inverter control system is not included since there is no difference. As shown in Table I, the proposed three-phase HFL-converter-based fuel cell system can achieve 3.9% higher capacitance reduction and better efficiency performance since the dc–dc converter soft switching operation can always be guaranteed. All those improvements are obtained by the proposed advanced phase shift and duty cycle control system based on the selected three-phase HFL converter.

IV. EXPERIMENTAL VERIFICATION

The experiments were conducted in the laboratory to verify the aforementioned theoretical analysis and the proposed direct double-frequency ripple current control performance. A 3.5-kW fuel cell system test bed was developed and is shown in Fig. 10. The size of the converter is 12 in $\times$ 10 in. The dc inductor and transformer designs in this paper adopt the planar cores with coils encapsulated within a multilayer printed circuit board. Both the LVS and HVS dc bus capacitors adopt the Epcos film capacitor as the energy buffer. The dc voltage source was used to emulate the steady-state characteristic of the fuel cell module. The three-phase HFL-converter-based fuel cell system test bed key circuit parameters are listed in Table II. The digital control board employs DSP TMS320F28335.

Figs. 11–13 show the experimental results with and without the proposed direct double-frequency ripple current control method. i_{ra}, $I_{\rm fc}$, V_d , $V_{\rm dc}$, and v_o represent the phase A secondary-side transformer current, fuel cell current, LVS dc-bus voltage, HVS dc-bus voltage, and inverter output voltage, respectively. Since the proposed fuel cell system has the high-frequency transformer, the synchronized soft start-up scheme presented in [32] and [33] is adopted to achieve the minimized transformer current response during the start-up transient.

Fig. 11 shows the baseline case I experimental results without the proposed method. In order to suppress the fuel cell current double-frequency ripple, the large electrolytic capacitors are connected to the HVS dc bus. The adopted capacitors for this case are the following: $C_p = 220\ \mu$F and $C_s = 3.18$ mF. As shown, $V_d = 51$ V, and $V_{\rm dc} = 200$ V, and they both have relatively very small ripple due to the relatively large capacitor. $i_{ra\_{\rm rms}} = 5.3$ A and $i_{ra\_{\rm peak}} = 11.4$ A. $v_o = 120$ V (RMS). $I_{\rm fc}$ average value is around 41 A.

Fig. 12 shows the baseline case II experimental results without the proposed method. The adopted capacitors for this case are the following: $C_p = 220\ \mu$F and $C_s = 180\ \mu$F. As shown in Fig. 12(a), $I_{\rm fc}$ contains the relatively large 120-Hz ripple current due to the relatively small capacitor. $\Delta I_{\rm fc}$ (peak to peak) $=$ 86.5 A. $\Delta V_{\rm dc} = 60$ V, and $v_o = 120$ V (RMS). $i_{ra\_{\rm rms}} =$ 7.1 A, and $i_{r\_{\rm peak}} = 20.2$ A. The transformer current has much larger RMS and peak values compared with Fig. 11 since the double-frequency ripple current is propagated into the fuel cell stack through the transformer. Fig. 12(b) shows the FFT analysis result of $I_{\rm fc}$ in Fig. 12(a). As illustrated, the 120-Hz component is 27.2 A, which is $27.2/41 = 66.3\%$ of the dc component. It further validates that $I_{\rm fc}$ has the relatively large double-frequency component. The $I_{\rm fc}$ shown in Fig. 12(a) contains the low-frequency harmonic. In addition, this harmonic frequency is 60 Hz, as shown in the FFT analysis result in Fig. 12(b).

Fig. 13 shows the experimental results with the proposed method. The adopted capacitors for this case are the following: $C_p = 220\ \mu$F and $C_s = 180\ \mu$F. As shown in Fig. 13(a), $I_{\rm fc}$

TABLE II
THREE-PHASE HFL-CONVERTER-BASED FUEL CELL SYSTEM TEST BED KEY CIRCUIT PARAMETERS

Three-phase HFL converter				H-bridge inverter	
Leakage inductor (μH)	Phase A: 1.10/Phase B: 1.10/Phase C: 1.11	DC inductor (μH)	Phase A: 14.64/Phase B: 14.65/Phase C: 14.72	L filter inductor (mH)	2.0
Transformer magnetizing inductor (mH)	Phase A: 0.11/Phase B: 0.09/Phase C: 0.12	Transformer turns ratio	4:16	Mosfets	Cree SiC CMF20120D
Primary-side Mosfets	IXFN320N17T2	Secondary-side Mosfets	Cree SiC CMF20120D	Anti-parallel Diode	Cree SiC C3D10060A
Primary-side film capacitor	Epcos 110 μF/450V ×2	Secondary-side film capacitor	Epcos 60 μF/800V ×3	Load	16.1 Ω
Switching frequency		40kHz		Switching frequency	20kHz

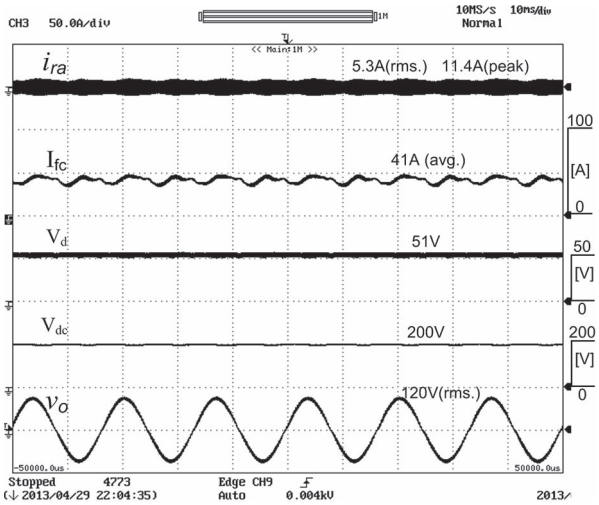

Fig. 11. Baseline case I: experimental results without the proposed control method, $C_p = 220\ \mu\text{F}$, $C_s = 3.18$ mF.

has the negligible low-frequency ripple. Therefore, it proves that the proposed method can almost eliminate the fuel cell double-frequency ripple with relatively small film capacitor. $v_o = 120$ V (RMS). $\Delta V_{\text{dc}} = 86$ V, and $\Delta V_d = 21$ V. As shown, the LVS dc-bus voltage V_d has been synchronized with V_{dc}. In addition, the voltage swing ratio $\Delta V_{\text{dc}}/\Delta V_d = 4.095$, which is very close to the transformer turns ratio 4.0. According to (A.1), the proposed varied duty cycle control with $d = 1$ is therefore validated. In addition, the result shown in Fig. 13(a) also demonstrates that the proposed direct-ripple current control and $d = 1$ control are perfectly decoupled as designed. $i_{ra\_\text{rms}} = 5.9$ A, and $i_{ra\_\text{peak}} = 13.7$ A. Compared with the results shown in Fig. 12(a), the transformer current has much smaller RMS and peak values since the double-frequency ripple current propagation path has been blocked. Compared with the results shown in Fig. 11, those two i_{ra_rms} values are very close. The i_{ra_peak} value is about 20% bigger with the proposed method. The dc-bus capacitance reduction is up to $(3.18 - 0.18)/3.18 = 94.3\%$ with the proposed method.

Fig. 13(b) shows the fast Fourier transform (FFT) analysis result of I_{fc} in Fig. 13(a). As illustrated, the 120-Hz component is almost zero, which further validates the performance of the proposed direct double-frequency ripple current control. The largest low-frequency ripple component is 60 Hz, and the magnitude is 2.5 A, which is only 6.1% of the dc component. The suggested ripple current is to be less than 10% of the dc component [26]. The control system is theoretically capable to mitigate this low-frequency component by adopting the multiple-resonant controller. However, it will increase the control system complexity. Since the ripple is within the limit, the multiple-resonant controller is not considered in this paper.

Fig. 14 illustrates the phase A LVS lower switch S_{a2} switching waveforms with fixed $D = 0.5$ control and $d = 1$ varied duty cycle control. The LVS lower switch switching waveforms are selected since their ZVS conditions are more critical compared with the LVS upper switches and HVS switches. This is caused by the effect of the dc inductor current [27]. For the test case shown in Fig. 14, $\varphi = 0.028\pi$, and $L_{\text{dc1}}/L_{s1} = 13.3$. Therefore, by calculation based on the ZVS conditions given in (A.2), the ZVS operation of S_{a2} requires $d < 1.07$. Fig. 14(a) shows S_{a2} switching waveforms with fixed $D = 0.5$ control. V_d is constant due to fixed D, and V_{dc} has the 120-Hz ripple due to the small dc-bus capacitance. As illustrated, two cases switching waveforms with maximum V_{dc} and minimum V_{dc} are highlighted. S_{a2} was hard switching with $d = 1.12$ at maximum V_{dc} and was soft switching with $d = 0.88$ at minimum V_{dc}. This result validated the ZVS conditions analysis. Fig. 14(b) shows S_{a2} switching waveforms with $d = 1$ varied duty cycle control. As shown, V_d was controlled to be synchronized with primary-referred V_{dc} for maintaining $d = 1$. Two cases switching waveforms with maximum V_{dc} and minimum V_{dc} are also highlighted. S_{a2} was soft switching in both cases. Therefore, it proves that the $d = 1$ varied duty cycle control can maintain ZVS operation of LVS lower switches.

Fig. 15 shows the three-phase HFL converter power loss breakdown analysis at rated load with assumed ZVS operation. As shown, the switching device conduction loss, the turn-off loss, and the inductor core loss are the three main losses. By comparing the results shown in Figs. 11 and 13, the I_{fc} and i_{ra} RMS and peak values are very close. Therefore, compared with the traditional method with large electrolytic capacitor, the switching device RMS current and turn-off current will not be increased too much if applying the proposed method with small film capacitor. The inductor core loss is mainly determined by the inductor current high-frequency ripple, which is not affected by the proposed method. In addition, the experimental results shown in Fig. 14 validated that the ZVS operation can be maintained with the proposed $d = 1$ varied duty cycle control. In conclusion, the proposed direct ripple current control method will not degrade the three-phase HFL converter operation efficiency.

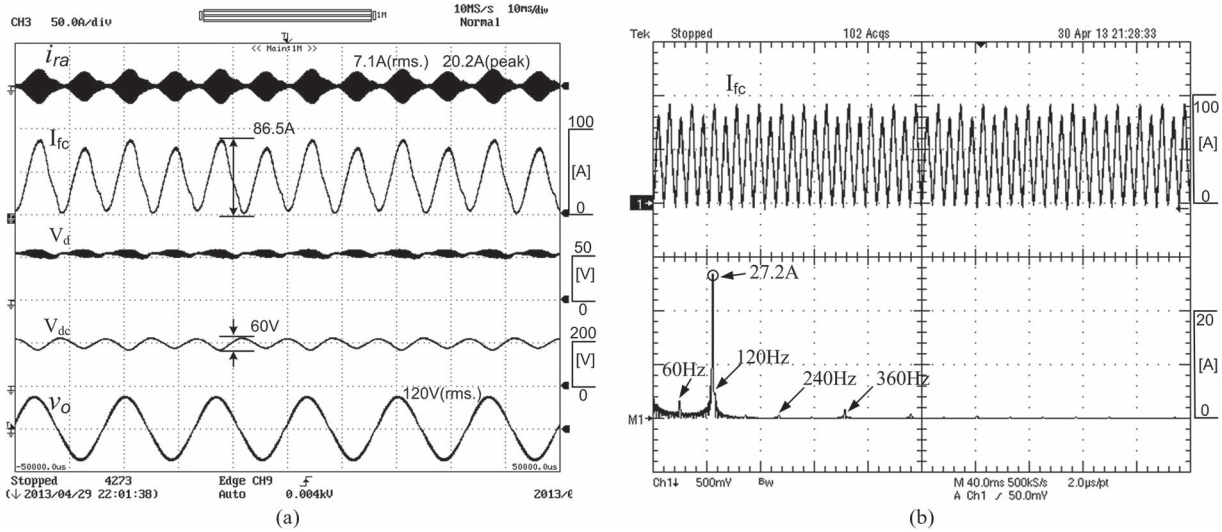

Fig. 12. Baseline case II: experimental results without the proposed control method, $C_p = 220\ \mu$F, $C_s = 180\ \mu$F. (a) System performance. (b) $I_{\rm fc}$ FFT analysis result.

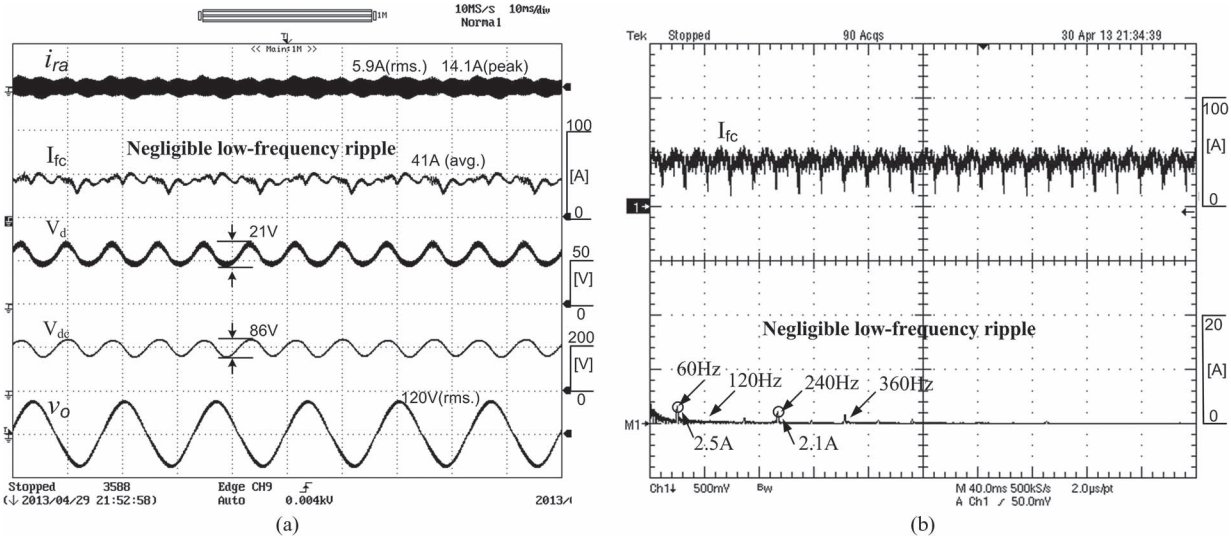

Fig. 13. Experimental results with the proposed control method, $C_p = 220\ \mu$F, $C_s = 180\ \mu$F. (a) System performance. (b) $I_{\rm fc}$ FFT analysis result.

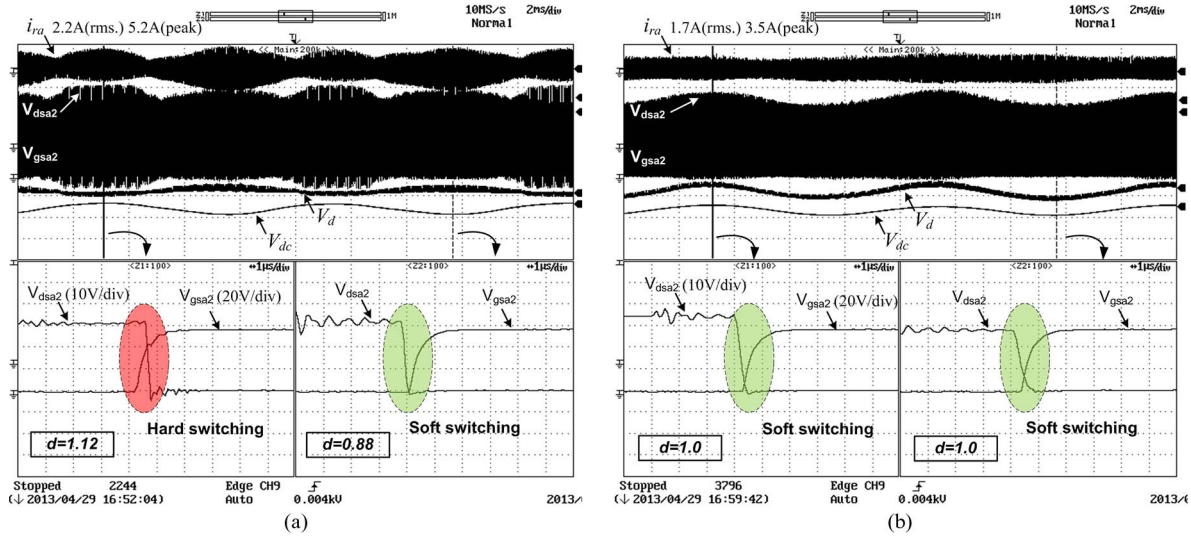

Fig. 14. Switch S_{a2} switching waveforms. (a) Fixed $D = 0.5$ control. (b) $d = 1$ varied duty cycle control.

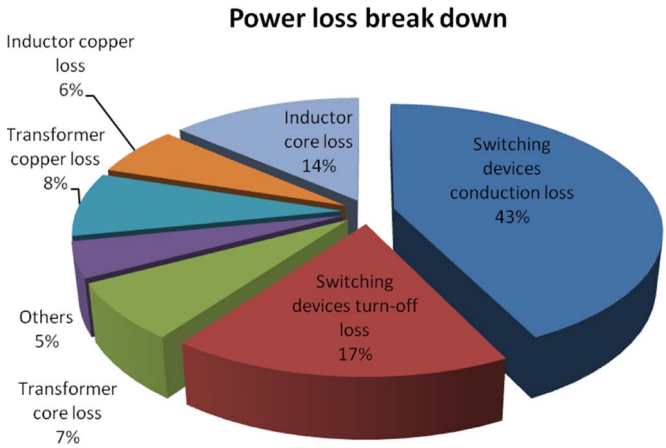

Fig. 15. Power loss breakdown analysis of the three-phase HFL converter with rated output power.

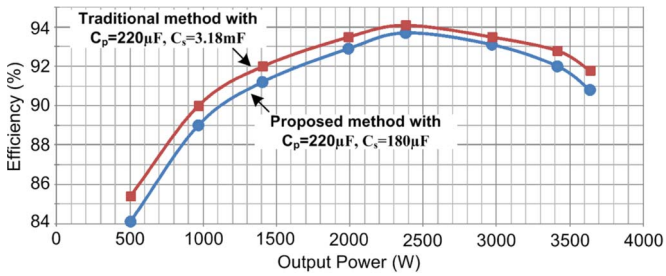

Fig. 16. Efficiency data comparison between the traditional method with large electrolytic capacitor and the proposed method with small film capacitor.

Fig. 16 shows the proposed fuel cell system efficiency data comparison between the traditional method with large electrolytic capacitor ($C_p = 220\ \mu$F, $C_s = 3.18$ mF) and the proposed method with small film capacitor ($C_p = 220\ \mu$F, $C_s = 180\ \mu$F). As shown, the system efficiency with the proposed method is very close to the one with the traditional method. The peak efficiency for the traditional method and the proposed method is 94.1% and 93.7%, respectively. The difference is only 0.4%. For rated load operation, the efficiency is decreased by 0.9%. This result is consistent with the results shown in Figs. 11 and 13 since the proposed method has about 20% larger transformer peak current.

V. Conclusion

This paper has proposed a three-phase HFL-based fuel cell power conditioning system that can achieve low-frequency ripple-free input current using a direct double-frequency ripple current control. The fuel cell system ripple circuit modeling has been presented to illustrate that the proposed method can make full utilization of capacitive ripple energy sources. The control system design based on the small-signal model has been analyzed in detail. To directly eliminate the fuel cell current double-frequency ripple, a PR controller is developed to achieve an extra high control gain at 120-Hz resonant frequency. This controller generates the virtual high impedance that can block the ripple energy propagation from inverter load to fuel cell stack, and it also eliminates the disturbance from varied duty cycle. The presented soft switching analysis shows that the proposed $d = 1$ varied duty cycle control can maintain all switching devices ZVS operation with large dc-bus voltage swing. The PR controller is adopted for duty cycle control in order to achieve the $d = 1$ operation and eliminate the inverter load current and phase shift variation disturbances. The experimental results validate the proposed technology performance, and the dc-bus capacitance reduction is up to 94.3% compared with the traditional method.

Appendix

$$d = \frac{N_p V_{\rm dc}}{N_s V_d} \tag{A.1}$$

where N_p and N_s are the transformer primary- and secondary-side turns ratios, respectively. V_d and $V_{\rm dc}$ are the LVS and HSV dc-bus voltages, respectively.

The ZVS conditions at $D = 0.5$ for phase A switches can be expressed as follows:

$$\begin{cases} S_{a1}: \ d < -\frac{8\pi^2+9\pi^2/\left(\frac{L_{\rm dc}}{L_s}\right)}{4(7\pi\varphi-2\pi^2-3\varphi^2)} \\ S_{a2}: \ d > \frac{8\pi^2+9\pi^2/\left(\frac{L_{\rm dc}}{L_s}\right)}{4(\pi\varphi+2\pi^2-3\varphi^2)} \\ S_{r1}: \ d < \frac{2\pi-3\varphi}{2\pi} \\ S_{r2}: \ d < \frac{2\pi-3\varphi}{2\pi} \end{cases} \tag{A.2}$$

$$P_o = \frac{dV_d^2\varphi(4\pi-3\varphi)}{6\pi\omega L_s} \tag{A.3}$$

$$1\text{ -p.u. base power}: \ P_{o\_\rm base} = \frac{V_d^2}{\omega L_s} \tag{A.4}$$

where P_o is the three-phase HFL converter output power. φ is the phase shift angle. ω is the switching angular frequency. L_s is the leakage inductor.

Choose $(i_a, v_d, v_{\rm dc})$ as state variables, $(v_{\rm in}, D, \varphi, i_{\rm dc})$ as control inputs, and $(i_a, v_{\rm dc})$ as controlled output. The average model state equation can be given as follows:

$$\begin{cases} L_{\rm dc1}\dfrac{di_a}{dt} = v_{\rm in} - Dv_d \\ C_p\dfrac{dv_d}{dt} = Di_a - \dfrac{V_{\rm dc}\varphi(4\pi-3\varphi)}{18\pi\omega L_{s1}} \\ C_s\dfrac{dv_{\rm dc}}{dt} = -i_{\rm dc} + \dfrac{V_d\varphi(4\pi-3\varphi)}{18\pi\omega L_{s1}}. \end{cases} \tag{A.5}$$

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Xiaohu Liu (S'09–M'13) received the B.S. and M.S. degrees from Huazhong University of Science and Technology, Wuhan, China, in 2007 and 2009, respectively, and the Ph.D. degree from Florida State University, Tallahassee, FL, USA, in 2013, all in electrical engineering.

He is currently an Electrical Engineer with the High Frequency Power Electronics Laboratory, GE Global Research Center, Schenectady, NY, USA. His research interests include topology and control of soft-switching dc–dc converters, magnetic resonance imaging gradient driver and power electronics applications in light-emitting diode drivers, solar microinverters, and fuel cell systems.

Hui Li (S'97–M'00–SM'01) received the B.S. and M.S. degrees from Huazhong University of Science and Technology, Wuhan, China, in 1992 and 1995, respectively, and the Ph.D. degree from The University of Tennessee, Knoxville, TN, USA, in 2000, all in electrical engineering.

She is currently a Professor with the Electrical and Computer Engineering Department, Florida A&M University–Florida State University College of Engineering, Tallahassee, FL, USA. Her research interests include bidirectional dc–dc converters, cascaded multilevel inverters, and power electronics applications in fuel cell systems and hybrid electric vehicles.